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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,556	03/12/2001	Jaroslav Hynecek	ISE103	9129

27382 7590 11/17/2005

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EXAMINER	
YODER III, CHRISS S	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,556	HYNECEK, JAROSLAV	
	Examiner	Art Unit	
	Chriss S. Yoder, III	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9* is/are rejected.

7)☒ Claim(s) *5-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed September 14, 2004 have been fully considered but they are not persuasive.

Applicant argues that Kaplan's patent is not relevant, since it does not show anywhere charge multiplication CCD stages between the CCD wells 14,16. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., charge multiplication CCD stages between the CCD wells) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant also argues that in FIG. 1 of Kaplan it shows that (24) is an amplifier, not a charge multiplier and that the charge multiplication stages are incorporated between the wells of a serial register. However, the examiner is interpreting the amplifier in Kaplan to be the equivalent of a charge multiplier since both multiply a signal in order to change the output. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the charge multiplication stages are incorporated between the wells of a serial register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are

not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant also argues that the Kaplan invention shows registers (14) located in the image sensing area (10) coupled to photodiodes (12), and that in applicant's invention the registers are not located in the image sensing area and are not coupled to photodiodes. However, the examiner points out that the claim does not state that the registers are separate from the image sensor or that they are not coupled to photodiodes.

Applicant also argues that in the Kaplan invention the charge is not transferred from one register to another, and moreover, it is not multiplied. However, the examiner disagrees, in Kaplan, the charge is transferred from one register to another (column 5, lines 1-8; the overflow charge is transferred from the first register 14 to the second register 16) and multiplied (column 4, lines 40-42).

Applicant argues that the charge amount is not increasing during the readout and transfer from one CCD well (16) to another CCD well (16) and to the amplifier AMP (25). In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the charge amount is increases during the readout and transfer from one well to another well and to the amplifier) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that in Kaplan the anti-blooming overflow gate (31) is located on the other side (above) the photo diodes, not in any serial register. However, the examiner has not relied upon the overflow gate (31) in the rejection, the overflow gate that the examiner has relied upon is overflow barrier (22) as can be seen in figure 3 as well as column 5, line 4.

Applicant argues that in the present invention there are no photodiodes adjacent to registers, that charge is not supplied to registers in parallel (vertical) direction, and that charge is transferred in the horizontal direction and register has charge multiplication stages incorporated between register wells. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no photodiodes adjacent to registers, that charge is not supplied to registers in parallel direction, and that charge is transferred in the horizontal direction and register has charge multiplication stages incorporated between register wells) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that in the present invention that as the amount of transported charge increases due to the multiplication process, CCD wells need to be made wider to accommodate larger amount of charge and that when the charge reaches the overflow area it overflows from one register to the other and further to an overflow drain while it is being transferred in the horizontal direction. As for the limitation that when the charge reaches the overflow area it overflows from one register to the other and further to an

overflow drain while it is being transferred in the horizontal direction, Kaplan does teach this in column 5, lines 1-8. As for the limitation of the amount of transported charge increasing due to the multiplication process before overflow from one register to another and transfer to an overflow, this limitation is not claimed. As for the limitation of CCD wells need to be made wider, Kaplan was not relied upon to teach this limitation.

Applicant also argues that in Kaplan there is no charge increase and the transfer of charge from one register to another is not expected during the horizontal charge transfer.

Applicant argues, with respect to claim 2, that Kaplan's invention charge is not transferred from one register to the other during the process of horizontal transfer to the detection node. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., charge is transferred from one register to the other during the process of horizontal transfer to the detection node) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that none of the references (Kaplan, Farrier, and Burt) explain that charge overflows from one register to the other due to one register being narrower and not being able to accommodate the transported charge. However, the examiner disagrees, Kaplan teaches that charge overflows from one register to the other due to

one register being narrower and not being able to accommodate the transported charge (column 5, lines 1-8).

Applicant argues, with respect to claim 3, that the present invention does not claim that the signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula. The examiner points out that this is the limitation as claimed in claim 3, and that if this reply is correct in the fact that the present invention does not make such a claim, then applicant should cancel claim 3.

Applicant argues that Kaplan does not include anywhere in its structure charge multipliers (24 and 26), and that it uses only charge detectors with amplifiers (24 and 25). The examiner points out that "charge multipliers (24 and 26)" was incorrectly reference before, and that it should read "charge multipliers (24 and 25)", and that charge amplifiers (24 and 25) are considered to be the charge multipliers.

Applicant argues that in Kaplan, the charge cannot overflow from one register to another during the horizontal transport to detection node and amplifier one stage at a time. In response to this argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., charge overflows from one register to another during the horizontal transport one stage at a time) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that there is no mention of charge multiplier in Burt's column 4, line 55, and that there are no charge multipliers in Burt's FIG. 1: 5 and 10. However, the examiner points out that although there is not mention of a charge multiplier in column 4, lines 55, it is mentioned in the lines following (column 4, lines 55-64) as cited in the previous rejection and has been pasted below:

> "To achieve multiplication of charge in each of the elements of the multiplication register 5, sufficiently high amplitude drive pulses are applied to control electrodes 10 to both transfer signal charge from one element to the next adjacent element in the direction shown by the arrow and also to increase the level of signal charge by an amount determined by the amplitude of the drive pulses."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplan (US Patent # 5,867,215).

2. In regard to claim 1, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture that incorporates charge multipliers (24), said image sensor including a first CCD register (14) adjacent to at least a second CCD register (16) and coupled to the said first register through a charge overflow barrier (22), where charge may overflow during transfer (column 5, lines 1-8).

3. In regard to claim 2, note Kaplan discloses the use of that the second adjacent CCD register collects overflow charge (column 4, lines 33-39; the overflow charge is

sent to the second CCD register, 16) and transports it to at least one detection node located in each register (column 4, lines 40-51; the transport of the signal from the CCD well to the amplifier is considered to be the equivalent of the detection node), and each charge detection node having charge conversion sensitivity that may be different for each node (column 5, lines 1-6; although not explicitly stated, it is inherent that the sensitivity changes with respect to the charge handling capabilities, and the CCD registers, 14 and 16, are of different charge handling capabilities).

4. In regard to claim 3, note Kaplan discloses that the signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula (column 5, lines 45-61).

5. In regard to claim 9, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture, said readout architecture incorporating charge multipliers (24 and 25), CCD registers (14 and 16), and a charge overflow device in at least one of its registers (22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent # 6,444,968) in view of Farrier et al. (US Patent # 6,392,260).

7. In regard to claim 4, note Burt discloses the use of a solid-state image sensor (2) having a readout architecture that incorporates charge multipliers (column 4, lines 55-64; and figure 1: 5 and 10), said image sensor including: a CCD register that incorporates at least one charge-multiplication device element in at least one stage (column 4, lines 55-64; and figure 1: 5 and 10). Therefore, it can be seen that the Burt device lacks the use of said at least one stage having a progressively wider width. Farrier discloses the use of a CCD register having a progressively wider width (column 7, line 66 – column 8, line 28; and figure 3: 110). Farrier teaches that the use of a progressively wider width is preferred in order to carry all the charge transferred without blooming (column 8, lines 25-28). Therefore, it would have been obvious to one of ordinary skill in the art to modify the Burt device to include the use of a progressively wider width as suggested by Farrier.

Allowable Subject Matter

8. Claims 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. As for claims 5, the prior art does not teach or fairly suggest the use of a solid-state image sensor having a readout architecture having a CCD register having a progressively wider width, wherein the width of the register and the number of charge multiplication elements varies according to a predetermined formula.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chriss S. Yoder, III whose telephone number is (571) 272-7323. The examiner can normally be reached on M-F: 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CSY
November 11, 2005

NGOC-YEN VU
PRIMARY EXAMINER